AMENDMENTS TO THE SPECIFICATION:

Page 3, amend the paragraph beginning at line 3 as follows:

The invention provides an efficient packing instruction that allows different portions of two input operand data words to be combined within a packed output data word using a single instruction. Furthermore, the invention provides a shift operand that allows one of the data words being packed to be selected from a variable position within its input operand data word in a manner that provides the ability to combine an additional data manipulation with the packing operation, e.g. one of the portions to be combined into the packed output data word may be multiplied or divided by a power of two at the same time that it is being packed together with another data word portion. This contrasts with a system which may only pack together data words from fixed positions within input operand data words. The invention ~~recognises~~recognizes that a packing operation is a relatively simple operation for the data path of a data processing system to perform and accordingly additional functionality may be added to the packing operation ~~utilising~~utilizing circuit elements already present within the data path and without introducing processing cycle time constraints.

Page 4, amend the paragraph beginning at line 1 as follows:

Viewed from another aspect the present invention provides a method of data processing, said method comprising the steps of decoding and executing an instruction that yields a value given by: selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn; selecting a second portion of bit length B

of said data word Rm subject to an arithmetic right shift specified as a shift operand within said instruction; and combining said first portion and said second portion to form respective different bit position portions of an output data word Rd.

Page 5, amend the paragraph beginning at line 30 and continuing to page 6, line 13 as follows:

Figure 2 illustrates an example data path 2 of a data processing system that may be used to implement the instruction of Figure 1. A register bank 4 holds 32-bit data words to be manipulated. Both the input operand data words stored in Rm and Rn are read from this register bank and the result data word is written back to register Rd in the register bank 4. The data path 2 includes a shifting circuit 6 and an adder circuit 8. The many other data processing instructions provided by the system ~~utilise~~utilize this shifting circuit 6 and adder circuit 8 in various different ways. Such a data path 2 is carefully designed so that the time taken for a data value to propagate through the shifting circuit 6 and the adder circuit 8 is well matched to the data processing cycle time. Efficient use of the hardware resources of the data path 2 is made in systems in which those resources are active for a high proportion of every data word propagating through the data path 2. A sign/zero extending and masking circuit 10 is provided in parallel with lower portion of the shifting circuit 6. A ~~multiplex~~multiplexer 12 is able to select either the output of the full shifting circuit 6 or the output of the sign/zero extending and masking circuit 10 as one of the inputs to the adder circuit 8. The other input to the adder circuit 8 is the input operand data word of Rn.

Page 7, amend the paragraph beginning at line 31 and continuing to page 8, line 13 as follows:

In operation, the unshifted input operand data word of Rn passes directly from the register bank 16 to the selecting and combining logic 22. In the case of instruction of Figure 3, the most significant 16 bits of the value of Rn are selected and form the corresponding bits within the output data word Rd. In the case of the instruction of Figure 4 it is the least significant 16 bits of the input operand data word of Rn that are selected and passed to form the least significant bits of the output data word Rd. The input operand data word of Rm passes through the full shifting circuit 18. In the case of the instruction of Figure 3, an arithmetic right shift of k bit positions ~~in~~is applied and then the least significant 16 bits from the output of the shifting circuit 18 are selected by the selecting and combining circuit 22 to form the least significant 16 bits of the output data word of Rd. In the case of the instruction of Figure 4, the shifting circuit 18 provides a left logical shift of k bit positions and supplies the result to the selecting and combining circuit 22. The selecting and combining circuit 22 selects the most significant 16 bits of the output of the shifting circuit 18 and uses these to form the most significant 16 bits of the output data word of Rd.